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(12) United States Patent Hiyoshi et al.

(54) SILICON CARBIDE SEMICONDUCTOR DEVICE

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(56) References Cited

U.S. PATENT DOCUMENTS

5,169,793 A 12/1992 Okabe et al. 5,464,992 A 11/1995 Okabe et al.

(Continued)

FOREIGN PATENT DOCUMENTS

H04-229661 A 8/1992 H07-249765 A 9/1995

JP

JP

(Continued)

OTHER PUBLICATIONS

International Search Report in PCT International Application No. PCT/JP2014/071173, mailed Oct. 21, 2014.

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(57) ABSTRACT

There is provided a silicon carbide semiconductor device allowing for increased switching speed with a simpler configuration. A silicon carbide semiconductor device includes: a gate electrode provided on a gate insulating film; and a gate pad. The gate electrode includes a first combtooth shaped electrode portion extending from outside of the gate pad toward a circumferential edge portion of the gate pad and overlapping with the gate pad at the circumferential edge portion of the gate pad when viewed in a plan view. A p+ region includes: a central portion overlapping with the gate pad when viewed in the plan view; and a peripheral portion extending from the central portion toward the outside of the gate pad, the peripheral portion being provided to face the first comb-tooth shaped electrode portion of the gate electrode with a space interposed therebetween.

5 Claims, 15 Drawing Sheets

